REMARKS

Claims 1, 3-6, 8, 10, 11, 13-16, and 23-28 are in the application. By this amendment claims 1, 3, 4, 6, 8, 10, 11, 13, 14, and 16 have been amended, new claims 23-28 have been added, and claims 2, 7, 9, and 12 have been canceled without prejudice. Claims 17-22 were canceled without prejudice in response to a requirement for restriction.

REJECTION OF CLAIMS 1-7, 9-13, AND 16 UNDER 35 U.S.C. § 102(b)

Claims 1-7, 9-13, and 16 were rejected under 35 U.S.C. § 102(b) as being anticipated by Sato, U.S. Patent No. 5,739,587. This rejection is respectfully traversed.

Sato teaches in column 4, lines 49-58, that the second embodiment is characterized by that further interlayer connection conductors 121 and 122 are disposed around the interlayer connection conductor 120 shown in FIG. 1. These conductors 120-122 function not only to electrically conduct the upper and lower electrode layers 100, 110, but also to provide a support between the upper and lower electrode layers 100, 10. Therefore, any crack will not be easily created in the interlayer insulation film 130 on bonding.

Sato teaches in column 4, lines 64-67, and continuing to column 5, lines 1-8, that the third structure (shown in FIG. 3) includes a semiconductor substrate 10, a SiO_2 film 20 formed over the semiconductor substrate 10 and a double-layer wiring structure formed on the SiO_2 film 20. The double-layer wiring structure includes upper and lower electrode layers 100, 110, a plurality of interlayer connection conductors 40-45, an interlayer insulation film 60 and another interlayer insulation film 70. The upper electrode layer 100 is connected to the bonding wire 140. Through holes into which the interlayer connection conductors 40-45 are embedded are required to have a sufficient diameter to completely receive the respective conductor, which is equal to about 1 μm.

Sato teaches in column 5, lines 60-67, and continuing to column 6, lines 1-4, that the structure of FIG. 23C provides support columns 9500a, 9500b formed by conductors to absorb the bonding impact, as shown in FIG. 25. Thus, a crack less tends to be created

in the interlayer insulation film (e.g., CVDSiO$_2$ film). According to the structure of Sato's invention, therefore, the bondability can be enhanced. More particularly, the distortion of the silicon oxide film having its hardness higher than that of the metal wiring layer is suppressed to reduce the creation of cracks in the silicon oxide film. This is effective against the pad peeling and enhances the bondability.

Sato teaches in column 6, lines 7-11, that when the interlayer connection conductors 41-46 and so on are orderly disposed into a matrix as shown in FIG. 4 of Sato, the layout density can be increased. Since the bonding impact is evenly absorbed by the respective conductors, a crack less tends to be created in the interlayer insulation film.

Sato teaches in column 6, lines 59-67, that in the structure shown in FIG. 10A, each of the top, intermediate and bottom electrode layers 510, 530, 550 has a lateral extension in a given direction so as to function as a connection wire to the internal circuit. However, Sato's invention is not limited to such an arrangement, but may have only one extension usable as a leading wire. Even if the top electrode layer has an extension functioning as a leading wire, the interlayer connection conductors 561-563 are required to ensure the good bonding.

Sato teaches in column 7, lines 3-11, that the structure of FIG. 11 is characterized by that interlayer connection conductors (606 and so on) in an interlayer insulation film 520 are disposed to be perfectly aligned with the respective interlayer connection conductors (616 and so on) in an interlayer insulation film 540. This provides the maximum mechanical strength. In some cases, however, interlayer connection conductors (586 and so on) may be slightly offset from interlayer connection conductors (596 and so on) with partial overlaps, as shown in Sato's FIG. 12.

Sato teaches in column 7, lines 26-45, that as shown in FIG. 15, first, an electronic circuit using MOS transistors is formed by forming gate electrodes 1580 and 1570 of polysilicon or the like and diffusion layers of impurity 1560, 1550, 1540, 1520 and 1500 on a semiconductor substrate 10. Second, contact holes are formed in an insulation film 20. Titanium (Ti) film 4000 and titanium nitride (TiN) film 4100 are sequentially deposited on the insulation film 20 through the overall surface thereof. The titanium (Ti) film functions to reduce the contact resistance while the titanium nitride (TiN) film functions to facilitate the embedment of tungsten (W) into the contact holes in

the following step. In FIG. 15, reference numerals 1561, 1530 and 1510 designate titanium silicide (TiSi) layers. A tungsten (W) layer 5000 is then formed, as shown in FIG. 16. Subsequently, the overall surface of the tungsten layer 5000 is etched through RIE to embed the tungsten material into the contact holes, as shown in FIG. 17. Thus, embedded tungsten layers 4200a, 4200b and 4200c are formed.

Sato teaches in column 7, lines 54-67, and continuing to column 8, lines 1-3, that aluminum (Al) and titanium nitride (TiN) layers are stackedly formed and worked through the conventional photolithography to form such electrodes as shown by 1210 and 1212; 110 and 112; and 1110 and 1112 in FIG. 18. The titanium nitride (TiN) film functions to prevent the reflection of exposure light, that is, as a reflection preventing layer.

An interlayer insulation film 60 is then formed and through holes are selectively formed through the interlayer insulation film 60, as shown in FIG. 19. The same production process as shown in FIGS 15-18 is made to form a second electrode layer. In FIG. 19, reference numerals 4000d, 4000e and 4000f denote titanium (Ti) films; 4100d, 4100e and 4100f titanium nitride (TiN) films; 4200d, 4200e and 4200h tungsten (W) layers; 1200, 100 and 1100 aluminum (Al) electrodes; and 1202, 102, 1102 reflection preventing layers of titanium nitride (TiN) film.

Applicants, on the other hand, teach on page 3, lines 27-34, and continuing to page 4, lines 1-8, a semiconductor component that includes a metallization system having a portion comprising a layer of metal with gaps or slots formed therein. This portion is also referred to as an input or input feeder portion. The input feeder portion is coupled to another portion of the metallization system that has a width less than or narrower than that of the input feeder portion. The portion having the narrower width is also referred to as a signal transmission or router portion. Optionally, the signal transmission portion is coupled to another feeder portion for further transmission of electrical signals in the semiconductor component. In an embodiment where the metallization system is used as a test structure, the signal transmission portion may be referred to as a test portion.

The gaps in the feeder portions are areas devoid of metal that serve as stress-induced void-inhibition features for inhibiting grain growth within the metallization system during operation. Grain growth inhibition inhibits the supersaturation of

vacancies and the resultant voiding in the metallization system. Inhibiting void formation mitigates an increase in the resistance of the metallization system and the formation of open circuits within the metallization system.

Accordingly, applicant's claim 1 calls for, among other things, forming a first portion of a metallization system above the semiconductor substrate, the first portion vertically spaced apart from the semiconductor substrate by a first distance, wherein forming the first portion includes forming a first layer of dielectric material over the semiconductor substrate, forming a first opening in the first layer of dielectric material, the first opening having a surface, wherein at least one dielectric protrusion extends from the surface of the first opening, forming a second opening in the first layer of dielectric material, the second opening having a surface, wherein at least one dielectric protrusion extends from the surface of the second opening, and forming an electrically conductive material in the first and second opening. Applicant's claim 11 calls for, among other things, forming a first portion of a conductive interconnect over the semiconductor substrate, the first portion having a width, wherein forming the first portion includes forming a first layer of dielectric material over the semiconductor substrate, forming a first trench in the first layer of dielectric material, the first trench having at least one dielectric pillar, forming a second portion of the conductive interconnect over the semiconductor substrate, the second portion having a width, wherein forming the second portion includes forming a second trench in the first layer of dielectric material, the second trench having at least one dielectric pillar, wherein the first and second trenches are laterally spaced apart from each other, and disposing a second electrically conductive material in the first and second trenches. At least these elements of applicants' claims 1 and 11 are not included in the relied on reference of Sato. Because all elements of applicants' claims 1 and 11 are not included in the relied on reference of Sato, the relied on reference cannot anticipate claims 1 and 11.

Claims 3-6, 8, and 10 depend either directly or indirectly from claim 1 and are believed allowable over the relied on reference of Sato for at least the same reasons as claim 1.

Claims 13 and 16 depend from claim 11 and are believed allowable over the relied on reference of Sato for at least the same reasons as claim 11. Claim 13 further

sets out that forming the third portion of the conductive interconnect comprises forming a second layer of dielectric material over the semiconductor substrate, the second layer of dielectric material between the semiconductor substrate and the first layer of dielectric material, forming at least one trench in the second layer of dielectric material, and disposing a third electrically conductive material in the at least one trench in the second layer of dielectric material to form a filled trench that serves as the third portion of the conductive interconnect. Claim 16 further sets out that forming the third portion of the conductive interconnect includes forming a second layer of dielectric material over the semiconductor substrate, wherein the first layer of dielectric material is between the semiconductor substrate and the second layer of dielectric material, forming at least one opening in the second layer of dielectric material, disposing a second electrically conductive material in the at least one opening in the second layer of dielectric material to form a filled opening that serves as the third portion of the conductive interconnect. At least these elements of applicants' claims 13 and 16 are not included in the relied on reference, further precluding anticipation of claims 13 and 16.

REJECTION OF CLAIM 8 UNDER 35 U.S.C. § 103(a)

Claim 8 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Sato, U.S. Patent No. 5,739,587 as applied to claims 1-7 and 9-16 above. This rejection is respectfully traversed.

Claim 8 depends from claim 1 and is believed allowable over the relied reference of Sato for at least the same reasons as claim 1.

ALLOWABLE SUBJECT MATTER

Claims 14 and 15 were objected to as being dependent on a rejected base claim, but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. Claim 14 has been amended to be in independent form including most of the limitations of claim 11 from which it depended. Claim 14 was inadvertently written to depend from claim 11 when it should have been

written to depend from claim 12. The amendments to claim 14 are believed to place claim 14, and claim 15 which depends from claim 14, in condition for allowance.

NEW CLAIMS 23-28

New claims 23-28 have been added to further claim applicants' invention. It is believed claims 23-28 do not add new subject matter and are fully supported by the application as filed.

CONCLUSION

No new matter is introduced by the amendments herein. Based on the foregoing, applicants believe that all claims under consideration are in condition for allowance. Reconsideration of this application is respectfully requested.

Respectfully submitted,

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